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Question Paper Code : 80571

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Fourth Semester

Electrical and Electronics Engineering

EE 8451 – LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

(Common to : Electronics and Instrumentation Engineering/ Instrumentation and Control Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Mention the types of IC.

2. What do you understand from the word 'monolithic'?

3. Define "Slew rate" in op-amp.

4. Define "Thermal drift" in op-amp.

5. Define "Cut off frequency" in Low pass filter.

6. Mention the drawback of weighted resistor DAC.

7. What is the function of phase detector in PLL?

8. Mention the applications of 555 timer.

9. What are various standard negative voltage regulator ICs?

10. List any two characteristics of IC voltage regulator.

PART B — (5 × 13 = 65 marks)

11. (a) Explain the Photolithography process with neat sketch in IC fabrication.

Or

(b) Discuss various IC capacitor fabrication techniques.

12. (a) With neat sketch explain the 3 input Non- inverting summing amplifier with a gain of 3.

Or

(b) Describe the working of summer and differentiator circuit with neat sketch.

13. (a) Explain the working of a Positive Clamper circuit and draw the output voltage waveform for positive and negative V_{ref} values.

Or

(b) Explain the operation of a monostable multivibrator using op-amp with neat sketch and waveforms.

14. (a) Briefly discuss the working of an Astable multvibrator using 555 timer and also draw the output voltage and capacitor voltage.

Or

(b) With neat sketch describe the working of VCO in PLL.

15. (a) Discuss the concept of voltage regulator and also explain how the fixed voltage regulator has been converted to variable voltage regulator?

Or

(b) Explain the working of a 723 IC voltage regulator with current limit and current boost circuits.

PART C — (1 × 15 = 15 marks)

16. (a) Find the output voltage *Vo* in the ideal opamp circuit shown in Fig.16 (a). Assume base-emitter voltage of 0.7 V and $\beta = 99$ of transistor $Q1$.

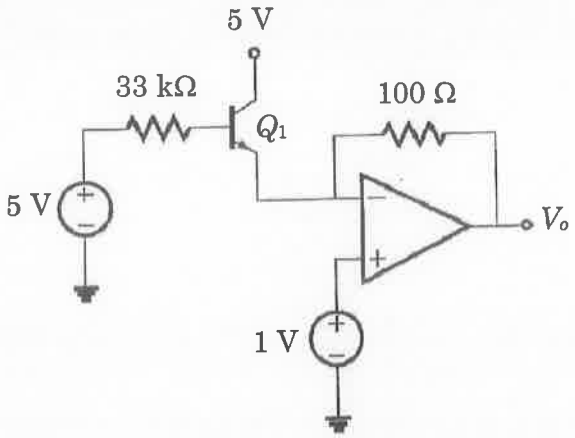

Fig. 16 (a).

Or

(b) Find the gain of the programmable gains amplifier shown in the following figure when S1 alone is closed, S2 alone is closed, S3 alone is closed, S4 alone is closed and both S1 and S3 is closed.

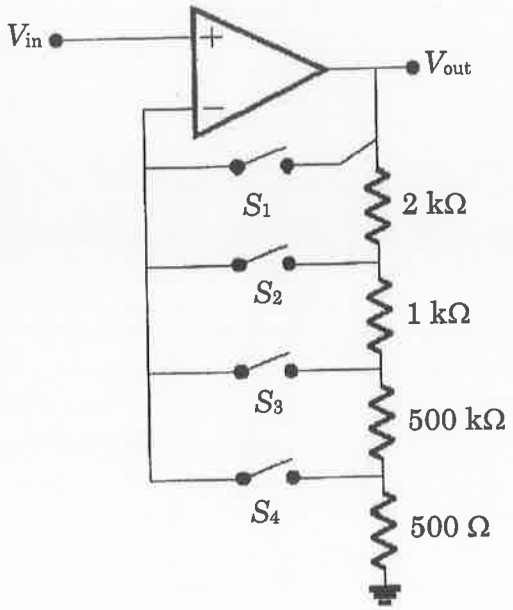

Fig.16 (b).